METHOD OF PLANARIZING A SEMICONDUCTOR DIE

is a continuation of US Application 10/423,270, filed on 04/25/03 and issued as US Patent 6,703,318; and

The present application claims the priority of a Provisional Application 60/422,314 filed on October 29, 2002, whose disclosure is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0001] The present invention relates to a method of planarizing a layer of a first material, and more particularly a dieletric layer, using chemical mechanical polishing techniques on a semiconductor die.

BACKGROUND OF THE INVENTION

[0002] Chemical mechanical polishing (CMP) is a well-known method to planarize a material used in semiconductor processing. Typically, the material to be planarized is a dieletric, such as silicon dioxide, which has been deposited on another dieletric such as silicon nitride. Further, the silicon nitride has a top planar surface with the silicon dioxide deposited thereon. However, because there are trenches in the substrate and with holes in the silicon nitride leading to the trenches, the silicon dioxide deposited on the silicon nitride will flow through the holes in the silicon nitride into the trenches in the substrate, thereby causing an uneven level above the top planar surface of the silicon nitride. Thus, the height of the silicon dioxide above the top planar surface of the silicon nitride can vary substantially. In the CMP method, it is desired to polish or remove the silicon dioxide so that it is planar with the top planar surface of the silicon nitride.

[0003] One prior art method to attempt to level the silicon dioxide is to create artificial dummy diffusion regions in the substrate of large field areas and filling it with oxide, but this does not address the large active areas and CMP's dishing effect associated with the large active areas. In other words, this method alone does not address the problem of the planarization of all the areas of the wafer. Another prior art solution is to mask certain portions of the silicon dioxide where the height of the silicon dioxide above the top planar surface of the silicon nitride is substantial. The silicon dioxide in the masked portion is removed thereby removing a substantial portion of the silicon dioxide in the portion where the height of the silicon dioxide above the top planar surface is substantial. This, however, creates a well-known undesired effect called "dishing" wherein polishing of the silicon dioxide causes the removal of silicon nitride in certain areas.